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Please find below and/or attached an Office communication concerning this application or proceeding.

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DETAILED ACTION

Response to Arguments

1. The Examiner considered the arguments presented by the Applicant discussing the proposed amendments on the claims but they are not found persuasive.

2. The Applicant argues the following:

a. Based on the results of the interview, independent claims 1, 8 and 12 have been amended to recite that "said second memory is always and only occupied by said second processing unit."

Furthermore, as discussed during the interview, support for these amendments can be found, at least, in Fig. 1 and paragraphs [0019], [0052], [0065], [0067], [0070] and [0076] of the publication of the present application (i.e., U.S. 2004/0187165). Specifically, the Applicants note that, for example, Fig. 1 illustrates that only the second processing unit 105 has access to the second memory 110. Furthermore, the Applicants note that paragraph [0052] states that the second processor 105 occupies the second memory 110, such that access to the second memory 110 cannot be interrupted by the main bus 101 [or any device communicating on the main bus]. The Applicants note that because the second memory is occupied only by the second memory, it would be understood by a person of ordinary skill in the art that the second memory is always and only occupied by the second memory.

- The Examiner would like to point out that, after careful analysis of the sections cited by the Applicant to provide support for the added limitations, the cited sections do not appear to provide support for the added wording "always and only" as added to the claims to indicate that said second memory is always and only occupied by said second processing unit.
- The following is an analysis of the cited section of the Specifications:

[**0019**] With this structure, since the second processing unit, which performs at least one of data processing and calculation in a larger amount than the first processing unit, uses the second memory, the second processing unit is released from contention of access to the first memory (*It is noted that this does not means that the second processing unit always and only use the second memory as claimed but only that the second processor uses it. Also does not mean that the first processor never uses the second memory. This section only appears to show that the second processor does not suffer from any delay caused by accessing the first memory*). That is, the second processing unit can process without latency time caused by the contention, and probability that the integrated circuit can complete processes to be done in real time increases (*The contention appears to be present if the second processor access the first memory as indicated in the previous sentence*).

[**0052**] In any case, a burden of the video processor 105 is heavier than that of the audio/multiplex/de-multiplex processor 106. That is, the video processor 105 should perform a larger amount of data processing and calculation

than the audio/multiplex/de-multiplex processor 106. Therefore, a local memory 110 is provided in the integrated circuit 100, and the video processor 105 occupies the local memory 110 (*It is noted that this section appears to describe that the second processor (105) uses more processing resources than the first processor (106) and thus, the second processor occupies the second memory (110). The Examiner understands that occupying a memory does not mean "always and only" occupying the memory as the Applicant argues. For example a memory could be occupied by a particular processor at a particular time and by another processor at another time. A memory could also be occupied by more than one processor. Therefore, the Examiner understands that one of an ordinary skill in the art would not reach the conclusion that the second processor always and only occupies the second memory because the second processor occupies the second memory considering the face that the word "occupy" does not require to "always and only occupy" as argues by the Applicant*).

[**0065**] When the video processor 105 receives the video signals, the video processor 105 expands the video signals using the local memory 110. Herein, since the video processor 105 occupies the local memory 110 and access of the video processor 105 to the local memory 110 is not interrupted by contention in the main bus 101, the video processor 105 can expand the video signals without delay (*This section appears to indicate that the second processor 105 uses the second memory 110 to expand the video signals while not being delayed by data from the bus 101. Thus it appears that during expansion of the video signals, the second processor may not be affected by data transmitted with the bus.*

However, although the second processor appears to be using or occupying the processor during the video expansion, the section does not require that the second processor 105 always and only occupies the second memory 110).

[**0067**] Next, operation when a bit stream is outputted will now be explained. First, when the camera 12 begins operation, image data obtained by the camera 12 is inputted into the image input circuit 13 of the video processor 105, the image input circuit 13 generates video signals, and the video processor 105 compresses the video signals using the local memory 110. Herein, since the video processor 105 occupies the local memory 110 and access of the video processor 105 to the local memory 110 is not interrupted by contention in the main bus 101, the video processor 105 can expand the video signals without delay (*Similar to ¶0065, this section appears to indicate that the second processor 105 compresses the video signal while not being interrupted by data from the bus 101. However, this does not require that the second processor 105 always and only occupies the second memory 110*).

[**0070**] While the audio/multiplex/de-multiplex processor 106 is performing some processes using the shared memory 104, the video processor 105 can perform the following processes using the local memory 110 without access contention (*This section appears to indicate that the second processor 105 can perform several processes without access contention. However, the section does not appear to indicate or suggest that the second processor 105 always*

and only occupies the second memory 110. Only that the second processor happens to be able to perform several processes using the second memory).

[**0076**] According to the present invention, since a processing unit, whose burden is heavy, occupies the second memory, avoiding latency time caused by contention of access to the shared memory or the first memory, probability that the integrated circuit 100 can complete processes to be done in real time increases (*This section appears to discuss that by having a processing unit that performs burdensome processing uses the second memory latency time causes by accessing the first memory is avoided and the process can be completed faster. However, this section does not require that the second processor 105 always and only occupies the second memory 110 as argued*).

The Examiner understands that although fig. 1 appears to show the memory 110 connected to the processor 105 (using arrows as shown in fig. 1), the representation in fig. 1 does not require that the memory 110 is always and only accessed by the processor 105 as argues. It merely shows a path between the processor and the memory. As explained above, the Specifications do not indicate that the memory 110 is always and only occupied by the processor 105.

Thus, the Examiner understands that the claims as amended are not supported by the Specifications, raising issues of new matter. Therefore, the proposed amendments will not be entered as they raise issues of new matter and also, issues that would require further search and/or consideration.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson D. Hernández Hernández whose telephone number is (571)272-7311. The examiner can normally be reached on 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/Nelson D. Hernández Hernández/
Primary Examiner, Art Unit 2622
September 21, 2011